The FSF-AD15000A is a single channel analog-to-digital conversion board based on two Analog Devices AD9625 single-channel, 12-bit, 2.5 GSPS ADCs.

**Product Outline**

The FSF-AD15000A is a single input analog-to-digital converter FMC, designed to be electrically and mechanically compatible with the ANSI/VITA 57.1 specification. Using two AD9625 ADCs clocked on opposite edges of a low jitter 2.5 GHz clock, a 5 GSPS interleaved data stream is produced.

The interleaving process results in unwanted spectral content due to imbalances that exist in all interleaved sampling systems (e.g. gain, phase, DC offset - both within and external to the ADCs). All of these factors have to be digitally reduced or cancelled, for the final 5GSPS stream to be of full value. Fidus can provide the interleaving compensation IP in addition to the hardware. This IP is fully functional in the demo .bit file, but ultimately times out.

**Features**

- Single input, 12-bit, 5 GSPS (equivalent) ADC in a double-width HPC FMC form-factor
- JESD204B Subclass 1 feature set including deterministic latency
- Designed for compatibility with ANSI/VITA 57.1
- Analog input bandwidth: 0.5 MHz – 3.3 GHz
- Extremely low phase noise onboard oscillator, with analog clock distribution topology for source phase-noise preservation
- External clock and trigger inputs
- Designed for experimentation, development, and integration into end systems
- 0 to +45°C operating temperature range*
- Xilinx® VC707 .bit file demonstration design
- Designed for compatibility with Xilinx® VC707 and VC709. Reference design available for VC707.
- ADC Multiple Device Synchronization (MDS) for coherent sampling across all ADC channels (JESD204B class MCDA-ML)
- Powered entirely through the FMC connector

* Components are rated from -40 to +85°C. Boards are only tested and characterized from 0 to 45°C.
Interleaving is also attainable because of the deterministic latency feature of JESD204B. Without deterministic latency, one would not be able to guarantee the desired 180° timing offset of the samples from each ADC. This feature ensures that across resets and power cycles, each interleaved sample is phased correctly.

JESD204B also offers benefits at the physical layer. Once sampled, the data from each ADC channel is transmitted on a high-speed serial bus to the downstream device. This serial data architecture minimizes downstream I/O pin count and increases performance by lowering system noise. Similarly, PCB layer count requirements are relaxed compared to a parallel or multi-lane LVDS data bus design. Essentially, the serial nature of JESD204B makes this design practical. The FSF-AD15000A requires a total of 16 multi-gigabit transceiver lanes (8 lanes per link), with each lane running at 6.25 Gbps, driving the need for a double width FMC.

Extra care has been incorporated in the design of the FSF-AD15000A to ensure extremely low jitter on the ADC sampling clocks. Low jitter performance is critical in preserving the full dynamic range of the converters when high frequency analog inputs are exposed to both wanted and unwanted wide dynamic range signals.

The FSF-AD15000A is an ideal starting point for broadband, high fidelity waveform digitization experimentation. It is also a great platform to get up and running quickly with a JESD204B interface. Finally, it serves equally well as a ready-made drop-in solution for end-systems that require high sample rate, high fidelity, waveform digitization.

Applications

General experimentation and instrumentation
Test and measurement (e.g. mass spectrometry)
Wideband Radar
Signals Intelligence (SIGINT)
## Typical Performance Characteristics

### Test conditions

Ambient Temperature: 25 ± 5°C, Host Platform: Xilinx VC707 Development Kit, RF Signal Generator w/ output filtering, Sample Clock: 2.5 GHz onboard oscillator, Interleaving and Interleaving Correction IP: Enabled, Forced Convection (bench top fan), Limited sample size to date

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Table 1: FSF-AD15000A Parameters
Other sample results

ADC Performance (Fin = 1575 MHz)
Demonstrates that the ADC performance on the FSF-AD15000A is comparable to Analog Devices’ published parameters for the individual AD9625-2.5. Also demonstrates that interleaving and interleaving correction does not negatively impact ADC performance.

Test conditions
Ambient Temperature: 25 ± 5°C, Host Platform: Xilinx VC707 Development Kit, RF Signal Generator w/ output filtering, Sample Clock: 2.5 GHz onboard oscillator, Interleaving and Interleaving Correction IP: Dependent on test, Forced Convection (bench top fan), Limited sample size to date

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Table 2: FSF-AD15000A ADC Performance Assessment at 1575 MHz
ADC Performance (Fin = 1800 MHz)

Demonstrates that the ADC performance on the FSF-AD15000A is comparable to Analog Devices’ published parameters for the individual AD9625-2.5. Also demonstrates that interleaving and interleaving correction does not negatively impact ADC performance.

Test conditions
Ambient Temperature: 25 ± 5°C, Host Platform: Xilinx VC707 Development Kit, RF Signal Generator w/ output filtering, Sample Clock: 2.5 GHz onboard oscillator, Interleaving and Interleaving Correction IP: Dependent on test, Forced Convection (bench top fan), Limited sample size to date

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<tr>
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<th>Typ</th>
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Table 2: FSF-AD15000A ADC Performance Assessment at 1800 MHz
ADC Performance (Fin = 2750 MHz)

Demonstrates that the ADC performance on the FSF-AD15000A at 2750 MHz.

**Test conditions**
Ambient Temperature: 25 ± 5°C, Host Platform: Xilinx VC707 Development Kit, RF Signal Generator w/ output filtering, Sample Clock: 2.5 GHz onboard oscillator, Interleaving and Interleaving Correction IP: Dependent on test, Forced Convection (bench top fan), Limited sample size to date

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<th>Typ</th>
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<td>Inter.=ON, Correction=OFF</td>
<td>25°C</td>
<td></td>
<td>40.0</td>
<td></td>
<td>dBC</td>
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<td></td>
<td>dBC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2750 MHz</td>
<td>Inter.=OFF, Correction=ON</td>
<td>25°C</td>
<td></td>
<td>dBC</td>
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</tr>
<tr>
<td>SPURIOUS FREE DYNAMIC RANGE (SFDR)</td>
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<tr>
<td>2750 MHz</td>
<td>ADI Datasheet Rev. A</td>
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<td></td>
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<td>25°C</td>
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<td>40.2</td>
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<td>dBC</td>
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<td>25°C</td>
<td></td>
<td>dBC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2750 MHz</td>
<td>Inter.=OFF, Correction=ON</td>
<td>25°C</td>
<td></td>
<td>dBC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EFFECTIVE NUMBER OF BITS (ENOB)</td>
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<td></td>
<td></td>
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</tr>
<tr>
<td>2750 MHz</td>
<td>ADI Datasheet Rev. A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>N/A</td>
</tr>
<tr>
<td>2750 MHz</td>
<td>Interleaving=OFF</td>
<td>25°C</td>
<td></td>
<td></td>
<td></td>
<td>Bits</td>
</tr>
<tr>
<td>2750 MHz</td>
<td>Interleaving Correction=OFF</td>
<td></td>
<td></td>
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<tr>
<td>2750 MHz</td>
<td>Inter.=ON, Correction=OFF</td>
<td>25°C</td>
<td></td>
<td></td>
<td></td>
<td>Bits</td>
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<tr>
<td>2750 MHz</td>
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<td>25°C</td>
<td></td>
<td></td>
<td></td>
<td>Bits</td>
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<tr>
<td>2750 MHz</td>
<td>Inter.=OFF, Correction=ON</td>
<td>25°C</td>
<td></td>
<td></td>
<td></td>
<td>Bits</td>
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</tbody>
</table>

Table 2: FSF-AD15000A ADC Performance Assessment at 2750 MHz
FSF-AD15000A performance w/ wideband noise

Demonstrates operation of the FSF-AD15000A and interleaving correction IP when challenged with a 60MHz wideband noise source.

**Test conditions**
Ambient Temperature: 25 ± 5°C, Host Platform: Xilinx VC707 Development Kit, RF Signal Generator w/ output filtering, Sample Clock: 2.5 GHz onboard oscillator, Interleaving and Interleaving Correction IP: Dependent on test, Forced Convection (bench top fan), Limited sample size to date

Interleaved ADC; Fin=1900MHz +/- 30MHz (60MHz wideband noise) with and without Interleaving Correction IP Enabled
### Interfacing and Integration

<table>
<thead>
<tr>
<th>Interface</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>FMC</strong></td>
<td></td>
</tr>
<tr>
<td>Connector type</td>
<td>HPC (High Pin Count Connector)</td>
</tr>
<tr>
<td>Voltage rails</td>
<td>12P0V, 3P3V, 3P3VAUX, VADJ (1.5-3.3V)</td>
</tr>
<tr>
<td>JESD204B data i/f</td>
<td>16x MGT data pairs (~6.25 Gbps each)</td>
</tr>
<tr>
<td>Analog Inputs</td>
<td>SMA, AC-Coupled, 50Ω, single-ended</td>
</tr>
<tr>
<td></td>
<td>0.5 MHz to 3300 MHz, +18 dBm FS</td>
</tr>
<tr>
<td>External Clock Input</td>
<td>SMA, AC-Coupled, 50Ω, single-ended</td>
</tr>
<tr>
<td></td>
<td>2500 MHz ± 1 MHz, +5 to +15 dBm</td>
</tr>
<tr>
<td>Trigger</td>
<td>SMA, DC-Coupled, ~4k to GND</td>
</tr>
<tr>
<td>Range</td>
<td>Single ended, (LV)TTL (3.6V max)</td>
</tr>
</tbody>
</table>

### Related offerings (additional charges and restrictions may apply)

<table>
<thead>
<tr>
<th>Part</th>
<th>Description</th>
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<tbody>
<tr>
<td>Native design files</td>
<td>Schematic, Layout, Artwork, Bill of Materials</td>
</tr>
<tr>
<td>FPGA code</td>
<td>Demonstration netlist or source code</td>
</tr>
<tr>
<td>FPGA IP core</td>
<td>FPGA IP core described below</td>
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<tr>
<td>Application code</td>
<td>Application source code for MicroBlaze®</td>
</tr>
<tr>
<td>Customization</td>
<td>Customization to fit individual needs</td>
</tr>
</tbody>
</table>

### Ordering Information

- 5GSPS, 12-bit ADC JESD204B FMC
  - PN: FSF-AD15000A
  - IP core: JESD204B w interleaver
  - PN: FSI-AD15000A-SRP

### Customization Services

Fidus is pleased to offer Hardware, Software, FPGA, Signal Integrity, and Mechanical services related to the integration and customization of this product.
FPGA IP

Fidus has completed the DSP work required to either reduce or cancel the spectral content that is related to the interleaving process. The following diagram depicts the FSI-AD15000A-SRP core.

Sales and Support
For additional information, questions or request for quotation visit: www.fidus.com

Customize your FS-AD15000A
Speak with our Design Services Group on how to accelerate your custom design: design@fidus.com

About Fidus
Fidus Systems, founded in 2001, specializes in leading-edge electronic product development with offices in Ottawa and Waterloo Ontario, and San Jose, California. Our hardware, software, FPGA and signal integrity teams architect, design and deliver next-generation products for clients in emerging technology markets. We build long-term relationships by consistently exceeding expectations.